



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:  
**30.08.2000 Bulletin 2000/35**

(51) Int Cl.7: **G11C 29/00**

(21) Application number: **99103478.6**

(22) Date of filing: **23.02.1999**

(84) Designated Contracting States:  
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU**  
**MC NL PT SE**  
 Designated Extension States:  
**AL LT LV MK RO SI**

(72) Inventors:  
 • **Huang, Shi-Yu**  
**Hsinchu, TW (TW)**  
 • **Kwai, Ding-Ming**  
**Hsinchu, TW (TW)**

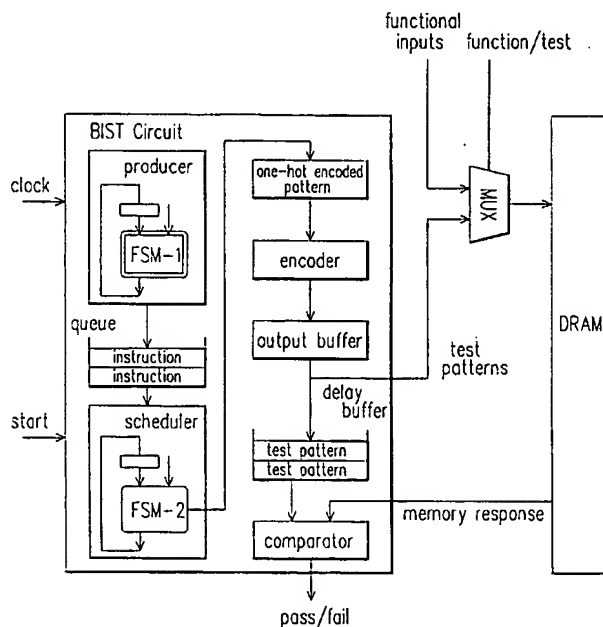
(71) Applicant: **Worldwide Semiconductor**  
**Manufacturing Corporation**  
**Hsinchu, TW (TW)**

(74) Representative: **Viering, Jentschura & Partner**  
**Postfach 22 14 43**  
**80504 München (DE)**

(54) **Built-in self-test circuit for memory**

(57) A built-in self-test (BIST) circuit and a method for testing a memory device, especially applicable in a DRAM requiring a complex test algorithm. Two finite machines are used instead of a single finite state machine used in the conventional circuit. Therefore, the pipeline technique can be applied to divide the test pattern gen-

eration process into stages, leading to a higher-speed design. In addition, a technique of protocol based relaxation is also presented. By imposing a certain protocol on the two communicating finite machines, the timing criticality is further relaxed. Synthesis results show that the proposed BIST circuit can operate at the speed of as high as 450MHz using 0.25µm CMOS technology.



**FIG. 3**

## Description

## BACKGROUND OF THE INVENTION

## 5 Field of the Invention

[0001] The invention relates to a test and a test hardware of a memory. More particularly, the invention relates to a built-in self-test circuit for memories embedded on the same chip.

## 10 Description of the Related Art

[0002] Memories are susceptible to fabrication process related failures caused by dust particles on the chips or masks, scratches and gate oxide pinholes, which may result open or short circuits. Many methods or hardwares have been developed to test whether a memory can function normally. However, as the integrated circuit art becomes more and more advanced, functions of memories become much more and more complex. Consequently, it often takes a great time and requires a complex circuit to perform a functional test of the memories.

[0003] Techniques of built-in self-test (BIST) for memories have been developed to resolve the above problems. In the built-in self-test technique for memory, a test algorithm is translated into a sequence of commands, data, and addresses applied to the memory under test. Traditionally, a hard-wired finite state machine (FSM) is used to implement the translation process. To provide the capability of at-speed testing, the BIST circuit operates as fast as the memory under test. A disadvantage of the approach is that the finite state machine is tailored to a specific set of test patterns whose complexity depends on the test algorithm. As the complexity of the test algorithm increases, this approach may be inadequate because the finite state machine may become too large and too slow to produce a test pattern in each clock cycle to intensively exercise the memory under test.

[0004] Some BIST circuits, known to be the programmable or configurable BIST circuits, can be referred to U.S. Patent No. 5,173,906, "Built-in Self-Test for Integrated Circuit" disclosed by Dreibelbis et al, in 1992. Another disclosure of a circuit that uses a micro-coded sequence defined in the contents of a read-only memory to produce the test patterns is issued with a US Patent No. 5,224,101 to Popyack et al in 1993. In US Patent No. 5,301,156, "Configurable Self-Test for Embedded RAMs", Talley et al discloses a circuit that has a serial path which passes through the address, command, and data portions of the circuit to shift in a test or control patterns and to shift out the results, each scan requiring several clock cycles.

[0005] The test algorithm for a dynamic random access memory (DRAM) is typically complex and requires a relatively long period of time to perform the test. In the above-mentioned prior art, none of them has disclosed a method nor a structure specially applicable in a DRAM to resolve the problem of testing speed.

## 35 SUMMARY OF THE INVENTION

[0006] The invention provides a circuit for memory testing, especially for a DRAM. The circuit comprises two finite state machines, so as to adapt the pipeline technique. In addition, a certain protocol on communicating these two finite machines is established. The timing criticality of the design is further relaxed.

[0007] The invention provides a built-in self-test circuit for testing a memory embedded on the same chip, especially for testing a DRAM. The built-in circuit comprises two finite state machines, a queue, an encoder, a memory input buffer, a delay buffer, and a comparator in a pipeline structure.

[0008] One of the finite state machines is called a producer which translates a test algorithm into a sequence of macro-instructions. The other finite state machine is called a scheduler which further interprets each of these macro-instructions into a series of test patterns. The queue is connected between the producer and the scheduler serving as a synchronization buffer, so that an operation of "latch-and-shift forward" is performed. The test patterns are then input from the scheduler to the encoder which encodes the test patterns from one-hot code into a binary code defined by the memory. The pipeline thus comprises three stages: the first stage translates the test algorithm into the macro-instructions, the second stage interprets the macro-instructions into the test patterns, and the third stage encodes the one-hot code into the memory defined binary code. Due to the potential performance degradation of the memory device introduced by the BIST circuit, the encoder is further connected to a BIST output buffer (BOB).

[0009] The delay buffer is connected between the BIST output buffer and the comparator. An expected response of memory is computed thereby.

[0010] The delay buffer outputs the computed result of the expected response to the comparator. The comparator then compares the expected response with the memory test response to determine whether the memory fails or passes.

[0011] The invention further provides a method for testing a memory, especially for testing a DRAM. A test algorithm is input and translated by a first finite machine into a sequence of macro-instructions. Being synchronized by a queue

according to a communication protocol, each of the macro-instructions is interpreted into a sequence of one-hot encoded test patterns. Each of the one-hot encoded test patterns is then mapped to a code defined by the DRAM. Via the BIST delay buffer, the mapped codes are fed into the DRAM to perform a test. As shown in the figure, a multiplexer (MUX) is further installed between the BIST circuit and the DRAM. The test results of both the output response of the DRAM and an expected memory response are input to the comparator. The comparator compares the output response of the DRAM with the expected memory response. While the test response of the memory appears the same as the expected response, the BIST circuit displays a "pass" information. On the contrary, if the test response of the memory is different from the expected response, the BIST circuit indicates a fail information.

**[0012]** It is to be understood that both the foregoing general description and the following detailed description are for exemplary and explanatory only and are not restrictive of the invention, as claimed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

##### **[0013]**

Figure 1 shows a state transition graph of march algorithm in the first finite machine;

Figure 2(a) shows a state transition graph for the second finite machine, wherein each node is a sub-machine;

Figure 2(b) shows the sub-machines for macro-instructions of READ\_A\_ROW, WRITE\_A\_ROW, and RWR\_A\_ROW;

Figure 3 is a block diagram of a built-in self-test circuit according to a preferred embodiment of the invention; and

Figure 4 shows a synchronization mechanism between the first and the second finite machines.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

##### The Test Algorithm

**[0014]** While performing a test on a memory device, a test algorithm written as a program in a high-level language is often proposed. Considering a DRAM comprising  $R$  rows and  $C$  columns is to be tested, four steps are included in a march algorithm. In a first step, '0' is written to every cell. The second step walks through the entire array in a forward manner, that is, from the first cell in the first row to the last cell in the last row. At each cell, a so-called READ(0)-WRITE(1)-READ(1) operation is performed. This READ-WRITE-READ operation is proposed in an attempt to better expose the potential dynamic defects of the memory cells. The third step walks through the entire cell from the last cell to the first cell. At each cell, a READ(1)-WRITE(0)-READ(0) operation is performed. The fourth step of this algorithm checks if the value of every cell is still zero after the first three steps.

**[0015]** An example of this march algorithm programmed in a high-level language is as presented herewith.

```

5      /*--- step 1: write 0 to each cell ---*/

10     foreach_row(i=0; i<R; i++){

        foreach_col(j=0; j<C; j++){Write 0 to cell(i, j)}

15     }

20     /*--- step 2: change each cell from 0 to 1 in a forward manner ---*/

25     foreach_row(i=0; i<R; i++){

        foreach_col(j=0; j<C;

30         Read 0 from cell(i, j)

35         Write 1 to cell(i, j);

40

45

50

55

```

**Read 1 from cell(i, j)**

5

}

10

/\*--- step 3: change each cell from 1 to 0 in a backward manner ---\*/

foreach\_row(i=R-1; i>=0; i--){

15

foreach\_col(j=(C-1); j>0; j--

20

**Read 1 from cell(i, j)**

25

**Write 0 to cell(i, j):**

**Read 0 from cell(i, j)**

30

}

35

/\*--- step 4: read 0 to each cell ---\*/

40

foreach\_row(i=0; i<R; i++){

foreach\_col(j=0; j<C; j++){ **Read 0 to cell(i, j)**}

45

}

50

}

55

The Macro-Instructions

**[0016]** In this invention, a pipeline comprising three stages for translating the high-level algorithm into test patterns for a memory device to be tested by a BIST circuit is disclosed. The algorithm is first translated into a sequence of

macro-instructions in the first stage, followed by further interpreting each of the macro-instructions into a sequence of test patterns in the second stage. The one-hot codes of the test patterns are then encoded into a binary code defined by the memory device.

[0017] In this embodiment, a DRAM is taken as an example to be tested. To test a DRAM, a basic activity often comprises at least one of the memory commands {*mem\_nop*, *mem\_active*, *mem\_read*, *mem\_write*, *mem\_precharge*, *mem\_refresh*} defined by the DRAM, where

*mem\_nop* performs no operation.

*mem\_active* activates the wordline of a row.

*mem\_read* issues a memory read command.

*mem\_precharge* bring voltages of columns to a precharge level.

The entire sequence of memory commands needed to complete a read/write cycle from a specific cell to another specific cell is called an operation, denoted as READ/WRITE. For example, a READ operation to a memory cell may be composed of the sequence of {*mem\_active*→*mem\_nop*→*mem\_read*→*mem\_read*→*mem\_nop*→*mem\_precharge*}. Apart from the above memory commands, a test pattern further comprises data value, row address, and column address.

[0018] The macro-instructions are expressed by four-tuples (opcode, data, row-address, column-address), where data, row address, and column address could be "Don't care" represented by "\*". Seven types of macro-instructions are used in the design:

(NOP, \*, \*, \*) corresponds to the test pattern (*mem\_nop*, \*, \*, \*).

(READ, *v*, *r*, *c*) reads an expected value *v* from the cell with row address *r* and column address *c*. This macro-instruction corresponds to a basic read cycle.

(WRITE, *v*, *r*, *c*) writes an expected value *v* from the cell with row address *r* and column address *c*. This macro-instruction corresponds to a basic write cycle.

(READ\_A\_ROW, *v*, *r*, \*) reads an expected value *v* from every cell in a row *r* sequentially.

(WRITE\_A\_ROW, *v*, *r*, \*) writes a binary value *v* from every cell in a row *r* sequentially.

(RWR\_A\_ROW, *v*, *r*, \*) performs the READ-WRITE-READ operation to every cell in row *r* sequentially. The three data values for the operation depends on the value of *v*. If *v* is 0, then READ(0)-WRITE(1)-READ(1) is performed. On the other hand, if *v* is 1, then READ(1)-WRITE(0)-READ(0) is performed.

(REFRESH\_A\_ROW, \*, *r*, \*) refreshes the contents of every cell in row *r*.

[0019] A detailed description of the march algorithm is given in this paragraph. Assume that the memory array under test has *R* rows and *C* columns. Fig. 1, Fig.2(a) and Fig. 2(b) respectively show the state transition graphs of the two finite machines for implementing the marching algorithm. Both machines operate along with an incrementer that keeps track of the row address and/or column address (represented by variables *row* and *col*). The first machine comprises four symbolic states excluding the *start* and *finish* states as shown in Fig. 1. Each transition may associate a trigger condition and an operation. The trigger condition is the condition that needs to be satisfied in order to exercise the associated transition, while the operation is the action to be taken with the transition.

[0020] For example, if the present state is the state labeled WRITE\_A\_ROW(0) and the row address is the last (that is, *row*=*R*-1), then the machine will take the transition labeled T1 and the following actions:

Produce a macro-instruction (WRITE\_A\_ROW, 0, *row*, \*).

Set the variable *row* to 0.

Go to the next state labeled RWR\_A\_ROW(0, 1, 1).

[0021] The second machine, as shown in Fig. 2(a) and Fig. 2(b), taking the macro-instructions generated by the first machine as input, is a hierarchical state machine with seven sub-machines. Each sub-machine is used to interpret one type of macro-instruction. For simplicity, only the three sub-machines needed for the march algorithm described above is shown (that is, READ\_A\_ROW, WRITE\_A\_ROW, and RWR\_A\_ROW). In a more sophisticated test algorithm of a  
 5 DRAM, for example, the commonly used row disturb algorithm, may need all macro-instructions.

#### The BIST Circuit

[0022] Fig. 3 shows a block diagram of a built-in self-test circuit for testing a memory according to a preferred embodiment of the invention. This built-in self-test circuit is particularly applicable for testing a memory requiring a complex test algorithm, for example, for testing a dynamic random access memory. The main objective of the BIST circuit is to translate a number of high-level abstract algorithms into a sequence of test patterns. In order to provide the capability of at-speed testing, the BIST circuitry needs to operate at least as fast as the memory device under test. However, as the complexity of the test algorithm grows, the single finite state machine may become too large, and thus too slow to  
 15 produce a test pattern for every clock cycle when applied to high-speed memory devices. Therefore, a pipeline technique is employed and a high-speed BIST architecture comprising dual finite state machines is provided in the invention.

[0023] As shown in Fig. 3, the BIST circuit comprises a first finite state machine, namely, a producer, a queue, a second finite state machine, also called a scheduler, an encoder, an (BIST) output buffer (BOB), a delay buffer, and a comparator. A pipeline technique is employed to construct the BIST circuit. There are three stages in this pipeline design, that is, a macro-instruction generation via the producer in the first stage, a macro-instruction scheduling via the scheduler in the second stage, and a memory command encoding via the encoder in the third stage. Between the  
 20 producer and the scheduler, a communicating protocol is established and will be described as follows.

[0024] While the producer receives a high-level test algorithm, the test algorithm is translated into a sequence of macro-instructions thereby. This is the first stage of a pipeline.

[0025] The second finite machine interprets each macro-instruction into a sequence of test patterns, in which memory command parts are one-hot encoded. This component, related to the interface with the memory device, forms the second stage of the pipeline.

[0026] The queue is preferably a first-in-first-out register, serving as a synchronization buffer connected between the first and the second finite machines. In general, the producer is capable of producing one macro-instruction every  
 30 cycle. However, the scheduler can take multiple clock cycles to complete the processing of a macro-instruction. Therefore, the producer may have to be stalled from time to time in order to avoid overloading the scheduler with excessive macro-instructions. Therefore, a simple master-slave synchronization mechanism is used, wherein the scheduler is the master which controls the action of the producer and the synchronization queue through a signal named 'next'. When the signal 'next' is low, the producer and the queue are frozen, that is, the value of every flip-flop of the queue remains unchanged regardless of the clocking. On the other hand, as the signal 'next' is raised to high, the current  
 35 macro-instruction produced by the producer is inserted to the queue at the specified clock edge. Meanwhile, the producer enters the next state to compute the next macro-instruction. In other words, when the signal 'next' is asserted, the queue performs a shift-forward operation and latches in a new instruction generated by the producer at the same clock cycle. On the other hand, if the signal 'next' is de-asserted, the queue performs no operation. Thus, the only operation associated with this queue is "latch-and-shift-forward".

[0027] The encoder is a piece of combinational logic that maps the encoding of each memory command in the test patterns output by the scheduler from one-hot to the one defined by the memory device. For example, if an input vector of the input test pattern is (00001, 0, 0, 0), where "00001" represents the one-hot code of a read memory command. Being processed by the encoder, this read memory command is encoded into a binary code of a read memory command  
 45 defined by the memory device to be tested by the BIST circuit.

[0028] The BIST output buffer is a register that serves as a buffer between the BIST circuit and the memory device. This buffer eliminates the potential performance degradation of the memory device due to the introduction of the BIST circuit.

[0029] The delay buffer, again, is a first-in-first-out register file between the BIST output buffer and the comparator. It is primarily for computing the expected responses of the read memory command. The number of clock cycle delays  
 50 from BIST output buffer to the comparator corresponds to the CAS-latency defined by the memory device.

[0030] The comparator is a piece of combinational logic that compares the output responses of the memory device with the expected values provided by the delay buffer. For example, if a test pattern (*mem\_read*, 1, 0, 0) is applied to the memory device and the CAS-latency is two, then two clock cycles later, the memory device is supposed to produce a '1' at the data output. Meanwhile, the same test pattern should arrive at the comparator through the delay buffer and  
 55 the data part '1' of the test pattern (*mem\_read*, 1, 0, 0), can be extracted as the expected value for the comparison.

## The Speed-Up Technique

[0031] In addition to the high performance design techniques, such as one-hot encoding and retiming, a technique called protocol-based relaxation to boost the BIST circuit speed is further proposed. This technique is based on an observation that, among the three stages, the timing critical paths are mostly the producer. To relax the timing criticality, the producer is transformed into a multi-cycle path component (that is, a component produces one result for every two clock cycles or more). Since scheduler controls the action of the producer, this can be achieved by modifying the scheduler. The modification needs to be done in such a way that the signal 'next' will not be raised to high for two consecutive clock cycles.

[0032] All the macro-instructions discussed earlier on take more than one clock cycle to execute NOP which originally corresponds to a single test pattern (*mem\_nop*, \*, \*, \*). In order to comply with the above protocol, the interpretation of this macro-instruction to two *mem\_nop* memory patterns, that is,

NOP=(*mem\_nop*, \*, \*, \*)→(*mem\_nop*, \*, \*, \*) The increase in test time due to this modification is negligible, while the performance of speedup is significant.

[0033] From the above introduction, the method and the BIST circuit for testing a memory device such as a DRAM can thus be briefly summarized as follows. While a test algorithm is input to the producer, the test algorithm is translated into a sequence of macro-instructions. Being synchronized by a queue according to a communication protocol, each of the macro-instructions is interpreted into a sequence of one-hot encoded test patterns. Each of the one-hot encoded test patterns is then mapped to a code defined by the DRAM. Via the BIST delay buffer, the mapped codes are fed into the DRAM for performing a test. As shown in the figure, a multiplexer (MUX) is further installed between the BIST circuit and the DRAM. The test result, that is, the output response of the DRAM is then input to the comparator, so does an expected memory response. The comparator compares the output response of the DRAM with the expected memory response. While the test response of the memory appears the same as the expected response, the BIST circuit displays a "pass" information. On the contrary, if the test response of the memory is different from the expected response, the BIST circuit indicates a fail information.

## Synthesis Results

[0034] The present invention has been implemented as a register transfer level (RTL) code. It is simulated with the functional model of the memory device under test to establish the confidence of its functional correctness. Synthesis tool, design compile, is used to convert this RTL code into a netlist and perform logic optimization using 0.25μm CMOS technology library. Static timing analysis tool, design time, shows that the clock cycle time is under 2.21ns. The timing-driven feature of a place-and-route tool, Apollo, is used to generate the layout. Post-layout timing check shows no timing violation under above clock cycle time. Based on these results, we thus can conclude the proposed BIST architecture in the invention has great potential to run as fast as 450MHz.

[0035] Other embodiment of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples to be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

## Claims

1. A built-in self-test circuit for a memory device, comprising:

a first finite machine, to translate an input test algorithm into a sequence of macro-instructions;  
 a second finite machine, to interpreting each of the macro-instructions into a sequence of one-hot encoded test patterns;  
 a first-in-first out register, to serve as a synchronization buffer between the first and the second finite machines;  
 an encoder, to map each of a plurality of one-hot codes of the one-hot encoded test patterns into a code defined by the memory device;  
 an output buffer, to serve as a buffer between the built-in self-test circuit and the memory device;  
 a delay buffer, for delaying an expected memory response; and  
 a comparator, to compare an output response of the memory device with the expected memory response provided by the delay buffer, so as to determine whether the memory device functions correctly.

2. The built-in self-test circuit according to claim 1, wherein the memory device comprises a dynamic random access memory.



3. The interconnect structure according to claim 1, wherein the sequence of macro-instructions are defined according to a sequence of memory commands defined by the memory device.
4. The built-in self-test circuit according to claim 1, further comprises a multiplexer between the built-in self-test circuit and the memory device.
5. The built-in self-test circuit according to claim 1, wherein the delay buffer comprises a first-in-first-out register.
6. A built-in self-test circuit for testing a DRAM, comprising:
  - a producer, to produce a sequence of macro-instructions from a test algorithm;
  - a scheduler, to translate each of the macro-instruction into a sequence of test patterns;
  - a queue, associated with a latch-and-shift-forward operation between the producer and the scheduler according to a master-slave synchronization mechanism, that is, while a signal 'next' is asserted by the scheduler, performing a shift-forward operation and latching a new macro-instruction generated by the producer at a same clock cycle, and performing no operation while the signal 'next' is de-asserted;
  - an encoder, to encode one-hot codes of the test patterns into binary codes defined by the DRAM;
  - a BIST output buffer, serving as a buffer for the binary codes which is then fed into the DRAM for performing a test;
  - a delay buffer, to delay an expected DRAM response according to the test patterns; and
  - a comparator, to compare an output response of the DRAM with the expected DRAM response provided by the delay buffer.
7. The built-in self-test circuit according to claim 6, wherein the sequence of macro-instructions is produced according to a sequence of memory command defined by the DRAM.
8. The built-in self-test circuit according to claim 6, wherein the one-hot codes are used for encoding states of the producer and the scheduler.
9. The built-in self-test circuit according to claim 6, wherein the one-hot codes are used for encoding outputs of the producer and the scheduler.
10. The built-in self-test circuit according to claim 6, wherein a three-stage pipeline is formed by the producer, the queue, the scheduler and the encoder.
11. The built-in self-test circuit according to claim 6, wherein the producer is a two-cycle path component or is to produce a macro-instruction every two clock cycles.
12. The built-in self-test circuit according to claim 6, wherein master-slave synchronization mechanism is used to design the scheduler without producing the macro-instructions in consecutive clock cycles.
13. A method for testing a memory device using a built-in self-test circuit, the method comprising:
  - translating a test algorithm into a sequence of macro-instructions according to a plurality of memory commands defined by the memory device;
  - translating each of the macro-instructions into a sequence of one-hot encoded test patterns which comprises data, address, and commands;
  - encoding a plurality of one-hot codes of the test patterns into binary codes defined by the memory device to perform a test on the memory device;
  - delaying an expected memory response corresponding to a CAS latency defined by the memory device; and
  - comparing the expected memory response with an output response of the memory device after being tested to determine whether the memory device functions normally.
14. The method according to claim 13, wherein a producer is used to generate the sequence of the macro-instructions.
15. The method according to claim 14, wherein a scheduler is used to translate each of the macro-instructions into the sequence of test patterns.

16. The method according to claim 15, wherein a queue is implemented to communicate the producer and the scheduler using a synchronization master-slave mechanism.

5 17. The method according to claim 16, wherein the scheduler performs as the master to control the queue and the producer as a slave.

18. The method according to claim 14, wherein the producer, the scheduler, and an encoder which performs the encoding steps construct a three-stage pipeline.

10 19. The method according to claim 13, wherein the memory device comprises a dynamic random access memory.

15 20. The method according to claim 13, wherein the memory device fails if the expected memory response is the same as the output response of the memory device after being tested, while the memory device passes if the expected memory response differs from the output response of the memory device.

15

20

25

30

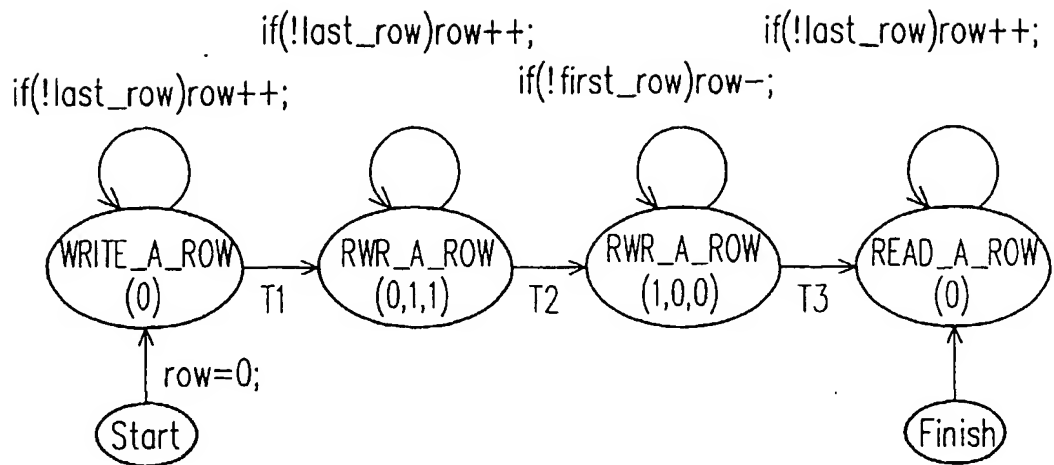
35

40

45

50

55



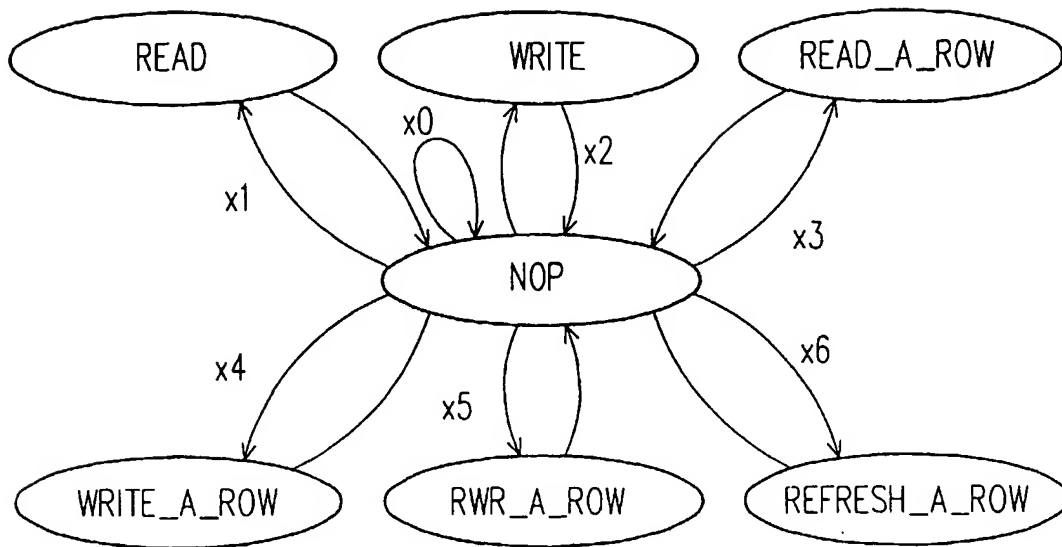
(Trigger conditions & actions for some labeled transitions)

T1: if(last\_row)row=0;

T2: if(last\_row)row=R-1;

T3: if(first\_row)row=0;

FIG. 1



(Trigger conditions of some labeled transitions)

x0: if(next-instruction==NOP)

x1: if(next-instruction==READ)

x2: if(next-instruction==WRITE)

x3: if(next-instruction==READ\_A\_ROW)

x4: if(next-instruction==WRITE\_A\_ROW)

x5: if(next-instruction==RWR\_A\_ROW)

x6: if(next-instruction==REFRESH\_A\_ROW)

FIG. 2(a)

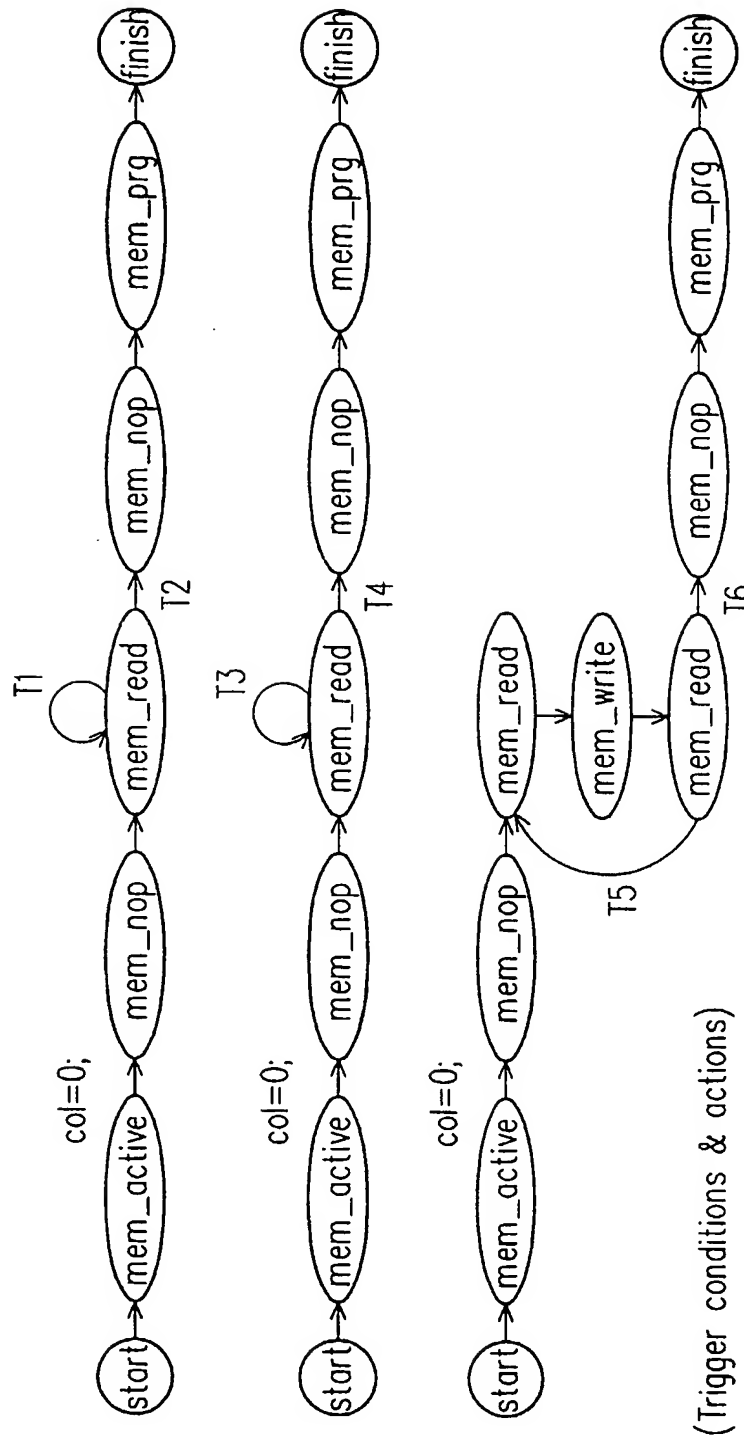


FIG. 2(b)

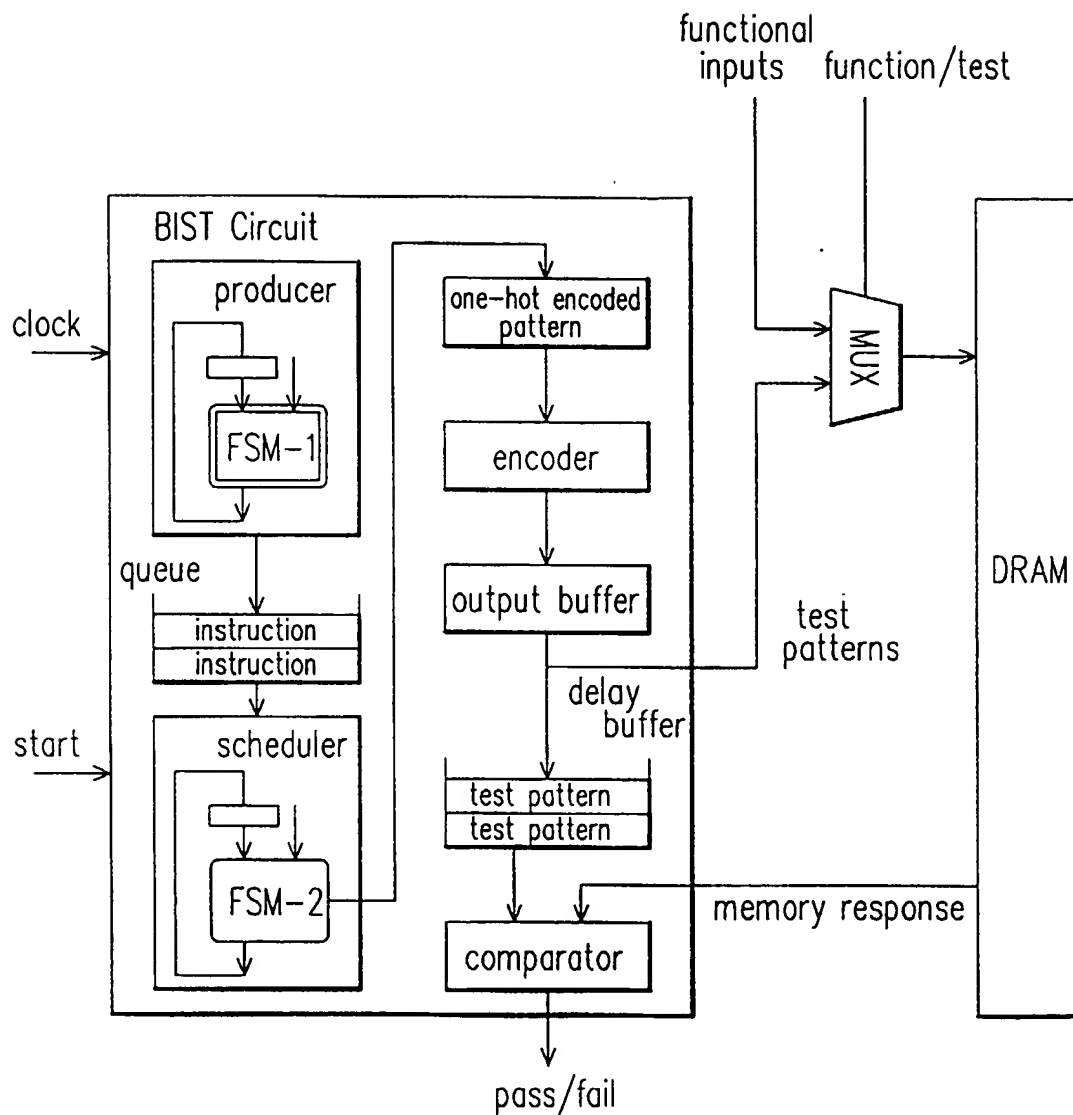


FIG. 3

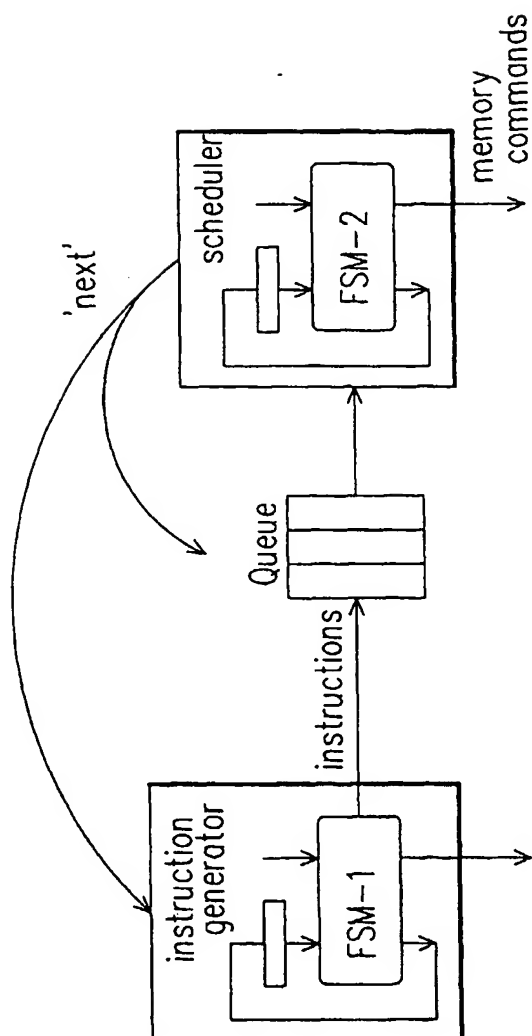


FIG. 4



European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 99 10 3478

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 3 831 148 A (GREENWALD D ET AL) 20 August 1974 * abstract; claims 1-11; figure 1 *	1-20	G11C29/00
A	EP 0 805 460 A (TEXAS INSTRUMENTS INC) 5 November 1997 * abstract; claims 1-6; figure 3 *	1-20	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G11C
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 21 June 1999	Examiner Sarasua Garcia, L
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... &amp; : member of the same patent family, corresponding document</p>			

EPO FORM 1503 03 82 (Pd/C01)



**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 99 10 3478

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.  
The members are as contained in the European Patent Office EDP file on  
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

21-06-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 3831148 A	20-08-1974	AU 476137 B	09-09-1976
		AU 6374373 A	19-06-1975
		CA 1012648 A	21-06-1977
		DE 2400010 A	04-07-1974
		FR 2212587 A	26-07-1974
		GB 1425110 A	18-02-1976
		JP 1136338 C	28-02-1983
		JP 49099447 A	19-09-1974
		JP 57016703 B	06-04-1982
		NL 7316504 A	04-07-1974
EP 0805460 A	05-11-1997	JP 10069799 A	10-03-1998

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82